



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,593	02/02/2004	Hamza Yilmaz	YMZ004 US	3820
34036	7590	07/19/2006	EXAMINER	
SILICON VALLEY PATENT GROUP LLP 2350 MISSION COLLEGE BOULEVARD SUITE 360 SANTA CLARA, CA 95054			MANDALA, VICTOR A	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 07/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

LC

<b>Office Action Summary</b>	<b>Application No.</b> 10/771,593	<b>Applicant(s)</b> YILMAZ, HAMZA	
	<b>Examiner</b> Victor A. Mandala Jr.	<b>Art Unit</b> 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 07 December 2005.  
 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.  
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-8 and 38 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
 6) ☒ Claim(s) 1,4,6 and 38 is/are rejected.  
 7) ☒ Claim(s) 1&38 is/are objected to.  
 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) ☐ All b) ☐ Some \* c) ☐ None of:  
 1. ☐ Certified copies of the priority documents have been received.  
 2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
 \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4, 6, and 38 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S.

Patent Application Publication No. 2004/084721 Kocon et al.

1. Referring to claim 1, Kocon et al. teaches a semiconductor device comprising: a semiconductor substrate, (Figure 8 #802), comprising a region of a first conductivity type, (Figure 8 #802 & 806), a top electrode, (Figure 8 #828), being in electric contact with a top surface of said substrate, (Figure 8 #802), a bottom electrode, (Figure 8 #830), being in electrical contact with a bottom surface of said substrate, (Figure 8 #802); a field shield region, (Figure 8 the bottom #814 p type), of a second conductivity type, said field shield region, (Figure 8 #814), being laterally bounded by dielectric sidewalls, (Figure 8 #816), said dielectric sidewalls, (Figure 8 #816), separating said field shield region, (Figure 8 #814), from said region of the first conductivity type, (Figure 8 #802 & 806), said field shield region, (Figure 8 #814), being bounded from below by a PN junction with said region of the first conductivity type, (Figure 8 #802 & 806); and a shield electrode, (Figure 8 #828), in electrical contact with the field shield region, (Figure 8 #814).

Art Unit: 2826

2. Referring to claim 4, Kocon et al. teaches a device of Claim 1 wherein the electrical contact between the top electrode and the top surface comprises a Schottky barrier, (Figure 8 #828).
3. Referring to claim 6, Kocon et al. teaches a device of Claim 1 wherein the electrical contact between the bottom electrode and the bottom surface comprises a Schottky barrier, (Figure 8 #830).
4. Referring to claim 38, Kocon et al. teaches a device of Claim 1 wherein the shield electrode, (Figure 8 #814), is in electrical contact with the top electrode, (Figure 8 #828).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S.

Patent No. 6,590,240 Lanois in view of U.S. Patent Application Publication No. 2003/0096464 Lanois.

5. Referring to claim 1, Lanois in view of Lanois teaches a semiconductor device comprising: a semiconductor substrate, (Figure 4 #1), comprising a region of a first conductivity type, (Figure 4 #2), a top electrode, (Figure 4 Portions of #6 disposed adjacent to #2), being in electric contact with a top surface of said substrate, (Figure 4 #1), a bottom electrode, (See \*\* below), being in electrical contact with a bottom surface of said substrate, (Figure 4 #1); a field

Art Unit: 2826

shield region, (Figure 4 #5), of a second conductivity type, said field shield region being laterally bounded by dielectric sidewalls, (Figure 4 #4), said dielectric sidewalls, (Figure 4 #4), separating said field shield region, (Figure 4 #5), from said region of the first conductivity type, (Figure 4 #2), said field shield region, (Figure 4 #5), being bounded from below by a PN junction with said region of the first conductivity type, (Figure 4 #2); and a shield electrode, (Figure 4 #6), in electrical contact with the field shield region, (Figure 4 #5).

\*\* Lanois ('240) does not illustrate a bottom electrode. However he teaches that "substrate 1 is intended for being a cathode contacting area of the diode" (Col. 2 Lines 31-34).

In a similar system Lanios (464) teaches placing a bottom cathode electrode 32 on the bottom of the substrate to allow the device to properly function as a diode.

It would have been obvious to one having skill in the art at the time the invention was made to have a bottom electrode on the system of (240) because (464) teaches it is required for the device to function properly as a diode.

6. Referring to claim 38, Lanois in view of Lanois teaches a device of Claim 1 wherein the shield electrode, (Figure 4 #5), is in electrical contact with the top electrode, (Figure 4 #6 and (240) shows that the portion of the electrode 6 above region 5 is connected to the portion of electrode 6 disposed adjacent to region 2).

#### ***Allowable Subject Matter***

7. Claims 2, 3, 5, and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Art Unit: 2826

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A. Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VAMJ  
7/9/06

  
**EVAN PERT**  
**PRIMARY EXAMINER**